LATTICE SEMICONDUCTOR CORP
Form 10-K/A
November 14, 2014
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UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549
FORM 10-K/A

(Amendment No. 1)
(Mark One)

[X] ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 FOR THE FISCAL YEAR ENDED DECEMBER 28, 2013

or

o TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

FOR THE TRANSITION PERIOD FROM TO
Commission file number: 000-18032

_____

LATTICE SEMICONDUCTOR CORPORATION
(Exact name of registrant as specified in its charter)

Delaware	93-0835214
(State of Incorporation)	(I.R.S. Employer Identification Number)
5555 NE Moore Court	
Hillsboro, Oregon	97124-6421
(Address of principal executive offices)	(Zip Code)

Registrant's telephone number, including area code: (503) 268-8000
Securities registered pursuant to Section 12(b) of the Act:

_____

(Title of Class)	(Name of each exchange on which registered)
Common Stock, $.01 par value	NASDAQ Global Select Market

Securities registered pursuant to Section 12(g) of the Act: None
Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes o No [X]
Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act.
Yes o No [X]
Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes [X] No o
Indicate by check mark whether the registrant has submitted electronically and posted on its corporate Web site, if any, every Interactive Data File required to be submitted and posted pursuant to Rule 405 of Regulation S-T (§232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit and post such files). Yes [X] No o
Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K (§229.405 of this chapter) is not contained herein, and will not be contained, to the best of the registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this

Form 10-K. [X]

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, or a smaller reporting company. See the definitions of “large accelerated filer”, “accelerated filer”, and “smaller reporting company” in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer o	Accelerated filer [X]
Non-accelerated filer o	Smaller reporting company o

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes o No [X]

Aggregate market value of voting stock held by non-affiliates of the registrant as of June 28, 2013	330,493,725
Number of shares of common stock outstanding as of November 11, 2014	118,033,629

DOCUMENTS INCORPORATED BY REFERENCE

The information required by Part III of this Report, to the extent not set forth herein, is incorporated herein by reference from the registrant's definitive proxy statement relating to the 2014 Annual Meeting of Stockholders, which definitive proxy statement was filed with the Securities and Exchange Commission on March 20, 2014.

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EXPLANATORY NOTE

Lattice Semiconductor Corporation (“Lattice” or the “Company”) is filing this Amendment No. 1 on Form 10-K/A to amend its Annual Report on Form 10-K for the year ended December 28, 2013, filed with the Securities and Exchange Commission (“SEC”) on March 11, 2014, solely to correct Exhibits 31.1, 31.2, 32.1 and 32.2. The remainder of the Annual Report on Form 10-K is included for convenience only and, except for corresponding updates to the cover page, Part IV and signature page, reflects the content of the Company's original Annual Report on Form 10-K for the year ended December 28, 2013, filed with the SEC on March 11, 2014. This Amendment No. 1 has not been updated to reflect any events occurring after the filing of the Company’s original Annual Report on Form 10-K for the year ended December 28, 2013, filed with the SEC on March 11, 2014.

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Forward-Looking Statements

This Annual Report on Form 10-K contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933, as amended, and Section 21E of the Securities Exchange Act of 1934, as amended. Any statements about our expectations, beliefs, plans, objectives, assumptions or future events or performance are not historical facts and may be forward-looking. We use words or phrases such as “anticipates,” “believes,” “could,” “estimates,” “expects,” “intends,” “plans,” “predicts,” “projects,” “may,” “will,” “should,” “continue,” “ongoing,” “future,” “potential” and phrases to identify forward-looking statements. Examples of forward-looking statements include, but are not limited to, statements about: our strategies and beliefs regarding the markets we serve or may serve; growth opportunities and growth in markets we may serve; acceptance of programmable logic devices and displacement of other general purpose logic solutions; our plans to introduce new FPGA families in high-growth market niches where we believe that we have sustainable and differentiated positions; the costs of making and developing various general purpose logic products; our intention to continually introduce new products and enhancements and reduce manufacturing costs; the majority of our revenue being through our sell-through distributors; the impact of our global tax structure and expectations regarding taxes and tax adjustments; our expectations that a significant portion of our revenue will continue to be dependent on the Consumer, Communications, Industrial, Scientific and Medical, and Computing end markets; the Asia Pacific market being the primary source of our revenue; our plans to sell our auction rate securities; the costs and benefits and timing of completion of our restructuring plans; the impact of new accounting pronouncements; our expectations regarding customer preferences and product use; our future product development and marketing plans; our ability to maintain or develop successful foundry relationships to produce new products; our expectations regarding seasonal trends; our expectations regarding defenses to claims against our intellectual property; our making significant future investments in research and development; our beliefs concerning the adequacy of our liquidity and facilities, and our ability to meet our operating and capital requirements and obligations.

Forward-looking statements involve estimates, assumptions, risks and uncertainties that could cause actual results to differ materially from those expressed in the forward-looking statements. The key factors that could cause our actual results to differ materially from the forward-looking statements include global economic conditions and uncertainty, the concentration of our sales in the consumer and communications equipment end market, particularly as it relates to the concentration of our sales in the Asia Pacific region, market acceptance and demand for our new products, any disruption of our distribution channels, unexpected charges, delays or results relating to our restructuring plans, the effect of the downturn in the economy on capital markets and credit markets, the impact of competitive products and pricing, unanticipated taxation requirements, or positions of the U.S. Internal Revenue Service, unexpected impacts of recent accounting guidance and the other risks that are described herein and that are otherwise described from time to time in our filings with the Securities and Exchange Commission, including, but not limited to, the items discussed in “Risk Factors” in Item 1A of Part I of this Report. You should not unduly rely on forward-looking statements because our actual results could differ materially from those expressed in any forward-looking statements made by us. In addition, any forward-looking statement applies only as of the date on which it is made. We do not plan to, and undertake no obligation to, update any forward-looking statements to reflect events or circumstances that occur after the date on which such statements are made or to reflect the occurrence of unanticipated events.

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PART I

Item 1. Business.

Lattice Semiconductor Corporation ("Lattice," the "Company," "we," "us," or "our") designs, develops and markets programmable logic products and related software. We also provide design services, customer training, field engineering and technical support.

Lattice was incorporated in Oregon in 1983 and reincorporated in Delaware in 1985. Our headquarters facility is located at 5555 N.E. Moore Court, Hillsboro, Oregon 97124, and our website is www.latticesemi.com. Information contained or referenced on our website is not incorporated by reference into, and does not form a part of, this Annual Report on Form 10-K. Our common stock trades on the NASDAQ Global Select Market under the symbol LSCC.

We report based on a 52 or 53-week fiscal year ending on the Saturday closest to December 31. Our fiscal 2013, 2012, 2011, and 2010 were 52-week years that ended December 28, 2013, December 29, 2012, December 31, 2011, and January 1, 2011, respectively. Our fiscal 2014 will be a 53-week year and will end on January 3, 2015. All references to quarterly or yearly financial results are references to the results for the relevant fiscal period.

Programmable Logic Market Background

Three types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic.

- Microprocessors are used for control and computing tasks.
- Memory is used to store programming instructions and data.
- Logic is employed to manage the interchange and manipulation of digital signals within a system.

Logic circuits are found in a wide range of today's digital electronic equipment, including communications, computing, consumer, industrial, scientific, medical, automotive, and military systems. The general purpose logic market for semiconductor solutions can be subdivided into three primary categories:

- Application-specific integrated circuits ("ASICs") are custom devices for a single user, which generally entail significant design risks, non-recurring expenses and longer development cycles. ASICs have historically been perceived as having advantages of lower unit costs, higher performance and lower power when compared to PLDs.
- Application-specific standard products ("ASSPs") are standardized logic devices marketed to multiple users, with limited flexibility to customize an end system. ASSPs have historically been perceived as having similar advantages as ASICs (ie: cost, performance and power) relative to programmable logic devices with the additional benefit of being readily available as an off-the-shelf standard product, thereby avoiding the risk and non-recurring engineering associated with ASICs.
- Programmable logic devices, including those offered by Lattice, are standard semiconductor products, purchased by systems manufacturers in a "blank" state that can be custom-configured into a virtually unlimited number of specific logic functions.

Industry sources have estimated that the general purpose logic and application-specific semiconductor product categories combined to account for approximately 37% of the estimated $318 billion worldwide semiconductor market in 2013. Based on those sources, we believe that the programmable logic market was approximately $4.5 billion in 2013.

Programmable logic devices have key competitive advantages over ASICs and ASSPs that make them suitable for certain types of applications, including:

- Faster time to market and increased design flexibility. These advantages are enabled by development software allowing users to implement and revise their designs quickly. ASICs and ASSPs, on the other hand, require significant development time and offer limited, if any, flexibility to make design changes.
- Programmable logic devices are standard components, meaning that the same device can be sold to many different users for a variety of applications, while ASICs and ASSPs are customized for an individual use or specific application.

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Programmable Logic Market

There are two main subcategories of programmable logic devices: field programmable gate arrays (“FPGAs”) and conventional programmable logic devices (“PLDs”), each representing distinctly different silicon architectural approaches.

- FPGAs are traditionally characterized by a narrow-input logic cell and use a distributed interconnect scheme. FPGAs may also contain dedicated blocks of fixed circuits such as memory, high-speed input/output interfaces or processors.
- PLDs are traditionally characterized by a regular building block structure of wide-input logic cells, called macrocells, and use a centralized logic interconnect scheme.

Although FPGAs and PLDs are typically suited for use in distinct types of logic applications, with PLDs being well-suited for 'control-oriented' applications and FPGAs being well-suited for 'data-path' applications, we believe that a substantial portion of programmable logic customers have needs for, and could utilize both FPGAs and PLDs. In addition, mixed signal programmable logic devices that combine digital and analog features are growing in popularity. We offer solutions utilizing all of these silicon architectures to serve multiple markets in a wide variety of applications. Throughout this Annual Report we generally use the term FPGAs when referring to both our FPGAs and our PLDs.

End Markets for Our FPGAs

An overview of the end market applications for our products is shown in the following table:

End Markets	Sub-Market	Applications	Tethered	Mobile
Communications	Wireless	Base Station	X	
		Wireless Backhaul	X	
		Heterogeneous Networks	X	
	Wireline	Routers and Switches	X	
		Data Centers	X	
		Carrier Class Wifi	X	
		Wired access aggregation	X	
Consumer		Smartphones		X
		Wearables		X
		Tablets & E-Readers		X
		Digital SLR Cameras		X
		GPS navigation units		X
		High Definition Televisions	X	
		Laptops and PCs	X	X
		Gaming	X	X
Industrial, Scientific and Medical (ISM)	Industrial	Factory Automation	X	X
		Motor and Process Controls	X	X
		Video Surveillance & Security	X	X
	Scientific	Human-Machine Interface	X	X
		Test and Measurement	X	X
	Medical	Diagnostic Imaging	X	X
		Hand-held Medical Devices	X	X
	Automotive	Driver Assistance Systems	X	X
		Driver Information Systems	X	X
Computing		Servers and Micro Servers	X	
		Data Centers	X	
		Storage networks	X	

	Security	X

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Lattice Strategy and Advantage

We believe that the number of devices that are always-on, always-connected and connected-to-everything (the "Internet of Things") which could benefit from our products will continue to expand, providing growth opportunities in many of the markets we serve today. Our strategy is to lead the middle-to-low-end of the FPGA market where high density, system-level integration, and the most advanced process technology are less necessary and to displace ASICs and ASSPs in applications where low cost, low power, small form factor, and rapid time to market are critical to the success of our customers.

The following table summarizes the key characteristics of our FPGAs relative to ASICs and ASSPs:

	Lattice FPGAs	ASICs/ASSPs
Time to Market	Fast	Slow
Development Cost (non-recurring engineering)	Lower	Higher
Customizable by User	Yes	No
Hardware Reprogrammability	Yes	No
Process Technology	Advanced	Often Lagging

We believe that the rapid pace of change and increasing complexity of products and connectivity places a premium on the programmable flexibility, rapid time to market, and relatively lower development costs and risks associated with our products when compared to ASICs and ASSPs.

Where time to market is critical to our customers, the reprogrammability of an FPGA solution allows designers to more quickly and simply add features, easily correct mistakes and/or fill gaps in other functions. Additionally, our focus on the development of customizable design solutions for our FPGAs ("IP Cores") provides customers with reliable, pre-tested, reusable functions that can be quickly adopted, allowing our customers to direct their time and energy on the unique aspects of their product. This can provide FPGAs a distinct time to market advantage over competing solutions.

Another advantage for certain of our FPGA solutions are their relatively advanced process technologies, often one or more generations ahead of competing ASICs, microcontrollers and ASSPs. This generational advantage from a lithography standpoint allows lower end FPGAs to compete directly on power and cost while offering a distinct advantage in form factor. We expect the fixed cost of ASIC and ASSP development to significantly increase on more advanced technology nodes, allowing FPGAs to better address high volume applications and gain market share from ASIC and ASSP suppliers.

The following table summarizes certain key characteristics of our FPGAs relative to higher density FPGAs offered by other FPGA companies:

	Lattice FPGAs	Higher Density FPGAs
Size	Smaller	Larger
Unit Cost	Lower	Higher
Power Consumption	Lower	Higher

Higher density FPGAs are large, expensive and consume greater power. Integrating multiple functions including high-end processors on a single device often requires expensive and advanced process technologies that lead to higher development and manufacturing costs. We have chosen not to compete at the high-end of this traditional FPGA market. Rather, we focus on providing more flexible solutions in the middle and low-end of the market by leveraging established process nodes to create multiple generations of cost effective devices on mature process technologies. By

leveraging established, lower cost t